WHAT IS CLAIMED IS:

1. A signal convertor for modulating or demodulating an input signal *x(t)*, comprising:

a synthesizer for generating wideband mixing signals φ_1 and φ_2, which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated;

a first mixer coupled to said synthesizer for mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal $x(t)\ \varphi_1$; and

a second mixer coupled to said synthesizer and to the output of said first mixer for mixing said signal $x(t)\ \varphi_1$ with said mixing signal φ_2 to generate an output signal $x(t)\ \varphi_1\ \varphi_2$.

2. The signal convertor of claim 1, where said synthesizer comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where φ_1 and φ_2 have different patterns.

3. The signal convertor of claim 2 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where neither φ_1 nor φ_2 have significant power at the frequency of said local oscillator signal being emulated.

4. The signal convertor of claim 3 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said input signal *x(t)* at baseband, thereby reducing adverse effects of local oscillator leakage.

5. The signal convertor of claim 4 wherein said synthesizer further comprises:

a synthesizer for generating mixing signals φ_1 and φ_2, where $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said input signal *x(t)* at baseband, thereby reducing adverse effects of local oscillator leakage.

6. The signal convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for randomly generating mixing signals φ_1 and φ_2.

7. The signal convertor of claim 1 wherein said synthesizer further comprises:

a synthesizer for pseudo-randomly generating mixing signals φ_1 and φ_2.

8. The signal convertor of claim 7 wherein said synthesizer further comprises: a synthesizer which can shape the spectrum of said mixing signals φ_1 and φ_2.

9. The signal convertor of claim 8 wherein said synthesizer further comprises: a delta-sigma block for generating said mixing signals φ_1 and φ_2.

10. The signal convertor of claim 9 wherein the control signal and oversampling rate of the delta-sigma block vary with time.

11. The signal convertor of claim 7 wherein said synthesizer further comprises: a synthesizer for generating mixing signals φ_1 and φ_2, where said mixing signals φ_1 and φ_2 can change with time in order to reduce errors.

12. The signal convertor of claim 7, further comprising: a filter for removing unwanted signal components from said *x(t)* φ_1 signal.

13. The signal convertor of claim 7, wherein said mixing signals φ_1 and φ_2 are digital waveforms.

14. The signal convertor of claim 7, wherein said mixing signals φ_1 and φ_2 are square waveforms.

15. The signal convertor of claim 7, further comprising: a local oscillator coupled to said synthesizer for providing a signal having a frequency that is an integral multiple of the desired mixing frequency.

16. The signal convertor of claim 7, wherein said synthesizer uses a single time base to generate both mixing signals φ_1 and φ_2.

17. The signal convertor of claim 7 wherein said synthesizer further comprises: a synthesizer for generating mixing signals φ_1 and φ_2, wherein φ_1 is at a much higher frequency than φ_2, thereby reducing the amount of 1/f noise in the output, at base band.

18. The signal convertor as claimed in claim 7, wherein said first and second time-varying signals are periodic functions of time.

19. The signal convertor as claimed in claim 7, wherein said synthesizer comprises:

a synthesizer for generating time-varying signals φ_1 and φ_2, where both φ_1 and φ_2 are operating at a much higher frequency than said local oscillator signal being emulated.

20. A signal convertor comprising two signal paths as claimed in claim 7, wherein said two sets of mixing signals are 90 degrees out of phase (φ_{1Q} and φ_{2Q} or φ_{1I} and φ_{2I}), thereby generating in-phase and quadrature components of said input signal x(t).

21. The synthesizer of claim 7 comprising:

one or more additional signal generators for producing one or more additional time-varying signals;

where the product of all of said time-varying signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said time-varying signals has significant power at the frequency of said local oscillator signal being emulated.

22. A method of converting the frequency of a signal *x(t)*, comprising the steps of:

generating wideband mixing signals φ_1 and φ_2, which vary irregularly over time, where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated;

mixing said input signal *x(t)* with said mixing signal φ_1 to generate an output signal *x(t)* φ_1; and

mixing said signal *x(t)* φ_1 with said mixing signal φ_2 to generate an output signal *x(t)* $\varphi_1 \varphi_2$.

23. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal $x(t)$, said synthesizer comprising:

a first signal generator for producing a first wideband mixing signal φ_1 which varies irregularly over time; and

a second signal generator for producing a second wideband signal φ_2 which varies irregularly over time;

where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated.

24. An integrated circuit comprising the device of claim 1.

25. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the device of claim 1.

26. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the device of claim 1.